SYSTEM FOR SYNCHRONIZING DISPLAY OF IMAGES IN A MULTI-DISPLAY COMPUTER SYSTEM

Inventors: Joseph P. Kennedy
John A. Klenoski
Greg Sadowski

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention is directed to synchronizing video and graphics images displayed on multiple display devices.

Related Art

[0002] Obtaining visual realism is crucial in computer graphics systems. To this end, it is often necessary to use multiple video or graphics processors to produce multiple levels of images on a single display device (e.g., a CRT, LCD, active matrix or plasma display). In the alternative, some video or graphics systems seek to achieve visual reality by generating a large visual image across multiple display devices. Each processor contributes to the overall image by providing a video or graphics signal representing, for example, either a front, left, or right view of the scene being displayed. Proper synchronization between the signals being provided to the various display devices is key to maintaining the reality of the scene being presented.

[0003] Several standards have been established that define various formats for video signals. The National Television Standards Committee (NTSC), Phase Alternate Line (PAL), and SEquential Couleur Avec Memoire (SECAM) are three widely accepted formats for television signals. Similarly, standards such as Video Graphics Array (VGA) and Monochrome Display Adaptor (MDA) are used to define display formats for computer displays. Depending on the standard used, a particular number of pixels, for example, 720, will be used to define a display or scan line. The scan lines are separated by synchronization pulses.

[0004] Horizontal synchronization (H-sync) pulses and Vertical synchronization (V-sync) pulses are two key components of the signals that are used to provide synchronization between multiple displays. These pulses represent the beginning of a new scan line in either the horizontal or vertical direction. When the horizontal or vertical synchronization pulses of the video signals generated by the participating processors are not aligned, visible distortions will be apparent.

[0005] Phase-locked loop (PLL) techniques are used to provide horizontal synchronization between multiple displays. Generally, these techniques phase-lock the horizontal synchronization pulse from a slave processor to the horizontal synchronization pulse of a master processor. A drawback to using a conventional phase-locked loop, however, is that the loop speed is fixed. A slow loop will be slow to adapt when the signals get out of synchronization. In contrast, a very fast loop will snap the signals into synchronization, often causing visible distortions or jitter in the display.

[0006] Vertical synchronization is usually achieved by resetting the vertical position of the slave processor upon the occurrence of a vertical reset in the master processor. In this way, vertical synchronization is achieved immediately. This process of "snapping" or causing the processors to become immediately synchronized with respect to their vertical positions also results in visible distortions.

[0007] Synchronization is made more difficult by the varying complexities of the images being presented on the various displays. As a result, many graphics systems will become desynchronized and/or produce visual artifacts or distortions in the resulting image. What is needed is a solution that will provide for vertical and horizontal synchronization of multiple displays while avoiding visual distortions.

BRIEF SUMMARY OF THE INVENTION

[0008] The invention is an image display system for synchronizing the display of images on a plurality of display devices. The system includes a first computer system generating a first signal representing first image data to be displayed on a first display device, a second computer system generating a second signal representing second image data to be displayed on a second display device, and means for synchronizing the first and second image data.

[0009] In a first embodiment of the invention, the computer system are arranged in a non-hierarchical configuration. A master sync signal is provided to both computer systems by a master sync signal generator or the like (which can be, for example, any video source). Each computer system includes synchronizing means that receives the master sync signal and causes the computer system to synchronize its output to this master sync signal.

[0010] Each synchronizing means includes a sync separator for receiving the master sync signal and producing a master pulse stream, a phase detector for comparing the master pulse stream to a slave pulse stream to produce a difference pulse stream, a low pass filter for filtering the difference pulse stream to produce an analog signal, a voltage controlled oscillator for producing a clock signal in response to the analog signal, and the digital rate controller. The digital rate controller divides the clock signal by a divisor value to produce the slave pulse stream and produces the divisor value based on a programmable rate value and a comparison of the master pulse stream and the slave pulse stream. A video generator generates a video signal based on the clock signal.

[0011] This second embodiment of the invention is adapted for synchronizing the display of video images generated by the two computer systems.

[0012] In a second embodiment, the computer systems are arranged in a master/slave configuration. In such a configuration, the first signal generated by the first computer system (i.e., the master) is used as a sync signal for the second computer system (and any other systems to be synchronized). The sync signal is

received by the synchronizing means in the second computer system. The synchronizing means includes a phase-locked loop (PLL) circuit having a digital rate controller to control a lock rate of the phase-locked loop circuit.

[0013] The synchronizing means includes a sync separator for receiving the first signal and producing a master pulse stream, a phase detector for comparing the master pulse stream to a slave pulse stream to produce a difference pulse stream, a low pass filter for filtering the difference pulse stream to produce an analog signal, a voltage controlled oscillator for producing a clock signal in response to the analog signal, and the digital rate controller. The digital rate controller divides the clock signal by a divisor value to produce the slave pulse stream and produces the divisor value based on a programmable rate value and a comparison of the master pulse stream and the slave pulse stream.

[0014] This second embodiment of the invention is adapted for synchronizing the display of computer graphics images generated by the two computer systems.

[0015] Another aspect of the invention is the phase-locked loop circuit having a digital rate controller. The digital rate control feature allows the phase-locked loop to be programmable so that its speed can be adjusted react more more quickly or more slowly to changes.

[0016] Further features and advantages of the present invention, as well as the structure and operation of various system and method embodiments of the present invention are described in detail below with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

[0017] The accompanying drawings, which are incorporated herein and form part of the specification, illustrate the present invention and, together with the description, further serve to explain the principles of the invention and to enable a person skilled in the pertinent art to make and use the invention. In the drawings, like reference numbers indicate identical or functionally similar

elements. Additionally, the left-most digit(s) of a reference number identifies the drawing in which the reference number first appears.

[0018] FIG. 1 is a diagram of a first embodiment of a multiple display computer system according to the present invention.

[0019] FIG. 2 is a diagram of a second embodiment of a multiple display computer system according to the present invention.

[0020] FIG. 3 is a schematic diagram of a video input/output module according to a first embodiment of the present invention.

[0021] FIG. 4 is a schematic diagram of an input/output (graphics sync) module according to a second embodiment of the present invention.

[0022] FIGS. 5A-5B illustrate an exemplary horizontal synchronization timing relationship between multiple displays.

[0023] FIGS. 6A-6C illustrate an exemplary horizontal synchronization timing relationship between multiple displays according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0024] As described above, some video or graphics systems seek to achieve visual reality by generating a large visual image across multiple display devices. In such systems, several video or graphics signals are being generated. To avoid the creation of visible distortions, proper synchronization between the video signals is critical.

[0025] In the case of video signals, the signals typically conform to a standard format. For example, each system could be configured to generate an image frame that is made up of 720 pixels per line. While the processors might each be generating 720 pixels per line, it is possible that they are not generating them at the same rate. Consequently, one processor might be at different point on the scan line than another. As a way of determining where each processor is with respect to processing a scan line, each processor provides a synchronization pulse, such as a horizontal or vertical synchronization pulse, to indicate the end of each

line. Visible distortions will be apparent when the horizontal or vertical synchronization pulses are not aligned. FIGS. 5A and 5B illustrate exemplary pulse streams that are not synchronized.

[0026] Referring to FIG. 5A, a pulse stream from a master processor (M) and a pulse stream from a slave processor (S) are shown. In this example, each system is shown generating pulse streams (from right to left) at a rate of 720 pixels per cycle. A horizontal synchronization pulse (H_{sync}) is added at the beginning of each new horizontal line. As is evident from the comparison of the two pulse streams shown in FIG. 5A, the slave processor is running faster than the master (i.e., the slave processor is issuing H_{sync} pulses ahead of the master processor when viewed from right to left in FIG. 5A). The difference in time is represented by the notation T_D. Similarly, in FIG. 5B, the master processor is shown running ahead of the slave processor. Consequently, visual distortions are likely to be apparent in the associated displays.

[0027] FIG. 1 is a diagram of a multiple display computer graphics system 100 according to a first embodiment of the present invention. The computer graphics system 100 has two or more computer processing systems 102. Two are depicted in this example, but system 100 can contain any number of computer processing systems. In this embodiment, computers 102 are arranged in a flat configuration (i.e., no hierarchical or master/slave type relationship).

[0028] Each computer 102 includes a central processing unit (CPU) 108, memory 104, a graphics processor 110, a monitor 114 and a display 116. Graphics processor 110 includes a clock 112. Each computer 102 also includes a video input/output (I/O) module 106. Graphics processor 110 receives graphics data from memory 104 under control of CPU 108 and displays graphical images on monitor 114. Video I/O module 106 receives video data from memory 104 under control of CPU 108 and displays video images on display 116.

[0029] In an example embodiment, monitor 114 is a cathode ray tube (CRT), LCD display, active matrix display, plasma display, or projector that displays data in a computer format such as VGA. Display 116 is a cathode ray tube (CRT),

LCD display, active matrix display, plasma display, or projector that displays video in a format such as NTSC, PAL, 720p x 1080i, or the like. By convention, the term "monitor" is generally used to refer to a device displaying computer data, while the term "display" is used to refer to a television or video type display device. As used herein, the term "display device" or simply "display" is used to refer to both monitors and displays unless otherwise indicated. In system 100, computers 102 each contribute to display of a video scene on displays 116.

[0030] Video I/O modules 106 receive a master sync (or master sync signal) from a master sync signal generator 101. Video I/O modules 106 then synchronize, to the master sync signal, output of the pixel and line based video signals to displays 116. The master sync signal may be any signal from which timing information can be extracted, such as, for example, a timing or clock signal or a video signal. The rate of the timing information extracted from the master sync signal determines the rate at which pixel information will be delivered to displays 116.

[0031] FIG. 3 is a schematic diagram illustrating the structure and operation of video I/O module 106. Video I/O module 106 includes a sync separator 302, a phase detector 304, a low pass filter (LPF) 306, a voltage controlled oscillator (VCO) 308, a video generator 310, and a digital rate controller circuit 314. Phase detector 304, LPF 306 and VCO 308 are elements of a conventional phase-locked loop (PLL).

[0032] Sync separator 302 receives the master sync signal (e.g., a video signal) and extracts a sync or master pulse stream 303. Video and other extraneous information are removed. Master pulse stream 303 represents horizontal sync pulses (i.e., line rate rather than pixel rate). Master pulse stream 303 is then provided to phase detector 304. Phase detector 304 compares master pulse stream 303 to a slave pulse stream 305 received from rate controller circuit 314 and generates a difference pulse stream having pulses of varying widths representing a difference between the compared signals. LPF 306 low-pass filters the difference pulse stream to produce an analog voltage. The analog voltage is then input to VCO 308, where it controls the oscillation frequency of the VCO.

The output of the VCO is a video clock signal 309 that is fed to video generator 310. Video clock signal 309 is also fed back to rate controller circuit 314.

[0033] Rate controller circuit 314 includes a rate controller 316, a programmable divider 318 and a digital comparator 312. Digital comparator 312 compares master pulse stream 303 to slave pulse stream 305 and produces a difference signal representing the lag or lead of slave pulse stream 305 with respect to master pulse stream 303. The difference signal is provided to rate controller 316. As explained in detail below, rate controller 316 is a programmable device that is software configurable. Rate controller 316 uses the difference signal (lead/lag information) and a programmable lock speed to generate a divisor value to programmable divider 318.

[0034] Programmable divider 318 is a countdown circuit. Starting with the divisor value from rate controller 316, divider 318 counts pulses in video clock signal 309 received from VCO 308 and decrements (counts down) the divisor value. When the countdown reaches zero, divider 318 produces an output pulse in slave pulse stream 305. In this countdown manner, divider 318 effectively implements a division operation. For example, if the divisor value is 720 (corresponding to 720 pixels per line), divider 318 will count 720 pulse in video clock signal 309 before issuing one pulse in slave pulse stream 305. This division converts a pixel count signal to a line count signal.

[0035] In one embodiment, rate controller 316 includes a programmable register and an adder/subtracter. Rate controller 316 may be programmed by placing in the register the programmable lock speed (i.e., a value that will control how fast or slow the phase-locked loop will respond to changes in the master sync signal). The lead/lag difference signal and the lock speed are then used by the adder/subtracter to produce the divisor value for programmable divider 318. In this manner, the divisor can be dynamically adjusted by rate controller 316 to control the speed or responsiveness of the phase-locked loop. The result is a loop that reacts quickly, but does not introduce jitter or other visual distortions or artifacts into the video signal.

[0036] In the 720 pixel per line example set forth above, rate controller 316 could initially set the divisor value to 720. If slave pulse stream 305 starts to lag master pulse stream 303, this will be detected by digital comparator 312 which would increase the value of the difference signal being provided to rate controller 316. In response, rate controller 316 will decrease the divisor to a value of, say, 710. This will cause pulses from divider 318 to arrive at phase detector 304 sooner than before. This, in turn, will cause VCO 306 to slow down, effectively decreasing the response time of the loop. Similarly, if slave pulse stream 305 starts to lead master pulse stream 303, this will be detected by digital comparator 312 which would decrease the value of the difference signal being provided to rate controller 316. In response, rate controller 316 will increase the divisor to a value of, say, 730. This will cause pulses from divider 318 to arrive at phase detector 304 later than before. This, in turn, will cause VCO 306 to speed up, effectively increasing the response time of the loop.

[0037] Conventional phase-locked loop circuits control loop speed by setting the cutoff frequency of LPF 306. Such a conventional circuit, however, is not adjustable, and the LPF must be set to either lock quickly (causes jitter), lock slowly (less jitter, but slow to respond), or a compromise setting between fast and slow. The present invention overcomes these deficiencies in conventional systems.

[0038] The resultant loop of the invention produces a stable video clock signal 309 that is synchronized with the master sync signal. Video generator 310 uses video clock signal 309 and video information from memory 104 (see FIG. 1) to produce the video signal that is provided to display 116. As would be apparent to a person skilled in the relevant art, video generator 310 includes appropriate video processing circuitry (not shown) including a frame buffer, pixel counter, line counter and associated circuitry.

[0039] FIG. 2 is a diagram of a multiple display computer graphics system 200 according to a second embodiment of the present invention. Computer graphics system 200 has a master computer processing system 202 and at least one slave

computer processing system 204. In this embodiment, computers 202 and 204 are arranged in a hierarchical or master/slave configuration. As with system 100, each computer 202,204 of system 200 includes a central processing unit (CPU) 108, memory 104, a graphics processor 110, and a monitor 114. Graphics processor 110 includes a clock 112. Computer 204 also includes an input/output (I/O) (graphics sync) module 206. Graphics processor 110 receives graphics data from memory 104 under control of CPU 108 and displays graphical images on monitor 114.

[0040] As would be apparent to a person skilled in the art, graphics processor 110 produces a display signal having a format appropriate for display on monitor 114. The display signal could be in a VGA format, for example. Each graphics processor (i.e., graphics accelerator or coprocessor) 110 may be any commercially available graphics processor such as the GeForce2 graphics processing unit available from Nvidia Corporation, Santa Clara, California, for example.

[0041] In the master/slave configuration of system 200, the display signal from graphic processor 110C of computer 202 (the master) is provided to computer 204 (the slave) to act as the master sync signal. I/O Module 206 of computer 204 (described in detail below) is similar to video I/O module 106 of system 100. I/O module 206 produces a clock signal 309 that is fed to clock 112D of graphics processor 110D to synchronize the output of graphics processor 110D of computer 204 to that of graphics processor 110C of computer 202.

[0042] FIG. 4 is a schematic diagram illustrating the structure and operation of I/O module 206. I/O module 206 is identical in structure and operation to video I/O module 106 discussed above, except that I/O module 206 does not include a video generator 310. Instead, clock signal 309 output by VCO 308 is fed directly to the clock 112D of graphics processor 110D.

[0043] Synchronization of two video signal according to the present invention is further illustrated below with reference to FIGS. 3 and 6. Referring to FIG. 6A, a master pulse stream (M) and a slave pulse stream (S) are shown. As is apparent by the time differential (T_D) between the horizontal synchronization pulses (H_{sync}),

the slave pulse stream (S) is five pixel pulses ahead of the master pulse stream (M). Referring to FIG. 6B, during a first iteration of the loop of I/O modules 106/206, slave pulse stream (S) is slowed by two pixel pulses. The time differential (T_D) between the H_{sync} pulses in the two pulse streams is now only three pulses.

[0044] Referring to FIG. 6C, during a next iteration of the synchronization loop, the slave pulse stream (S) is slowed by three pixel pulses. The time differential (T_D) between the H_{sync} pulses in the two pulse streams is now zero. By gradually bringing the master and slave pulse streams into synchronization in this manner, visual distortions are minimized. As compared to the invention, conventional systems would either (1) respond too slowly to an out-of-sync condition, or (2) would snap the slave pulse stream into synchronization with the master pulse stream, causing a visual distortion.

[0045] An advantage of the present invention is that the convergence time (i.e., how quickly the slave pulse stream can be synchronized to the master pulse stream) can be programmably adjusted via rate controller circuit 314. That is, the amount of time (i.e., in pixel pulses) added to (or removed from) the slave pulse stream during each iteration of the loop will determine how quickly the loop converges and achieves synchronization. For gross adjustments, the loop may be adjusted more coarsely (i.e., more pulses added/removed during each loop iteration) when the signals are grossly out of synchronization, and more finely (i.e., fewer pulses added/removed during each loop iteration) when the signals are closer to being synchronized. This produces a dynamically self-adjusting, phase-locked loop that is quick to respond, but stable enough to prevent visual distortions.

[0046] The present invention has been described in a multi-display computer system wherein one computer drives each display. In other embodiments, however, a single computer may have multiple processors, wherein each processor generates video and/or computer graphics images for a corresponding display device. Moreover, each computer described herein may be, for example,

a general purpose computer such as a personal computer, workstation or mainframe, or may be a special purpose computer such as a video player, game console, or the like. One skilled in the relevant art will recognize other arrangements that can benefit from, without departing from the scope of, the present invention.

[0047] In one embodiment, the invention is implemented primarily in firmware and/or hardware using, for example, hardware components such as application specific integrated circuits (ASICs). Implementation of a hardware state machine to perform the functions described herein will be apparent to a person skilled in the relevant art. In another embodiment where the invention is implemented using software, the software may be stored in a computer program product and loaded into computer systems 102, 202 and/or 204 via a network connection or via computer readable media such as a diskette, CD, DVD, or ROM device. The control logic (software), when executed by the one or more processors 108, causes the processor(s) 108 to perform the functions of the invention as described herein.

[0048] Various embodiments of the present invention have been described above. It should be understood that these embodiments have been presented by way of example only, and not limitation. It will be understood by those skilled in the relevant art that various changes in form and details of the embodiments described above may be made without departing from the spirit and scope of the present invention as defined in the claims. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.